What is claimed is:

1. A semiconductor chip, comprising:

a semiconductor substrate;

a functional bump provided on a surface of the semiconductor substrate for electrical connection between an internal circuit provided on the semiconductor substrate and a solid device; and

a dummy bump provided on the surface of the semiconductor substrate and not serving for the electrical connection between the internal circuit and the solid device.

2. A semiconductor chip as set forth in claim 1, wherein the dummy bump is a stress relieving bump for relieving a stress applied thereto.

3. A semiconductor chip as set forth in claim 1, wherein the dummy bump is a dummy bump formed in the same step of a production process as the functional bump.

4. A semiconductor chip as set forth in claim 1, wherein the functional bump is provided in an active region formed with a functional device, and the dummy bump is provided in a peripheral region surrounding the active region.

5. A semiconductor chip as set forth in claim 1, wherein the functional bump is provided on a peripheral portion of a mating surface of the

semiconductor chip opposed to the solid device,

wherein the dummy bump is provided on a central portion of the mating surface.

6. A semiconductor chip as set forth in claim 5, wherein the dummy bump has a greater contact area in contact with the solid device than the functional bump.

7. A semiconductor chip as set forth in claim 1, wherein the dummy bump is connected to a low impedance portion.

8. A semiconductor chip as set forth in claim 7, wherein the low impedance portion is the semiconductor substrate.

9. A semiconductor chip as set forth in claim 8, wherein the semiconductor substrate has a low resistance portion to be connected to the dummy bump, the low resistance portion having been subjected to a resistance reducing process.

10. A semiconductor chip as set forth in claim 8, wherein the dummy bump is connected to a scribe line region of the semiconductor substrate.

11. A semiconductor chip as set forth in claim 10, wherein the dummy bump is comprised of a plating-metallization layer formed on a seed layer provided on the surface of the semiconductor substrate, and the seed layer has an interconnection extending from

the dummy bump to the scribe line.

12. A semiconductor chip as set forth in claim 1, wherein the semiconductor substrate is covered with a planarized surface protective film, on which the functional bump and the dummy bump are provided as projecting therefrom.

13. A semiconductor chip as set forth in claim 12,

wherein the functional bump is electrically connected to an internal interconnection via an opening formed in the surface protective film,

wherein the dummy bump is formed on the surface protective film as electrically isolated from the internal circuit.

14. A semiconductor chip as set forth in claim 13, wherein the surface protective film is formed with a recess having a depth which corresponds to a distance between a surface of the surface protective film and the internal interconnection, and the dummy bump is provided on the recess.

15. A semiconductor chip as set forth in claim 13, wherein the dummy bump is provided on a recess formed in the surface protective film, and the recess has a depth which is determined so that the dummy bump has substantially the same projection height as the functional bump with respect to a surface of the surface

protective film.

16. A semiconductor chip as set forth in claim 13, wherein the internal interconnection has a surface portion which is exposed through the opening and is flush with the surface protective film, and the functional bump is provided on the exposed surface portion.

17. A semiconductor chip which is to be bonded to a surface of a solid device via a connection member for electrical connection between an internal circuit thereof and the solid device, the semiconductor chip comprising:

a dummy bump provided on a surface of the semiconductor chip opposed to the surface of the solid device and not serving for the electrical connection between the internal circuit of the semiconductor chip and the solid device;

wherein the dummy bump has a height determined on the basis of a distance defined between the surface of the solid device and the surface of the semiconductor chip by the connection member.

18. A semiconductor chip as set forth in claim 17, further comprising a surface protective film covering the surface of the semiconductor chip,

wherein the dummy bump is provided on a recess formed in the surface protective film.

19. A semiconductor device, comprising:

a solid device;

a semiconductor chip mounted and bonded onto a surface of the solid device;

a functional bump for electrical connection between an internal circuit of the semiconductor chip and the solid device; and

a dummy bump not serving for the electrical connection between the internal circuit and the solid device.

20. A semiconductor device as set forth in claim 19,

wherein the functional bump is disposed in association with an active region of the semiconductor chip formed with a functional device,

wherein the dummy bump is disposed in association with a peripheral region surrounding the active region.

21. A semiconductor device as set forth in claim 19,

wherein the functional bump is disposed in association with a peripheral portion of a mating surface of the semiconductor chip opposed to the solid device,

wherein the dummy bump is disposed in association with a central portion of the mating surface.

22. A semiconductor device as set forth in claim 20, wherein the dummy bump has a greater contact area in contact with the solid device than the functional bump.

23. A semiconductor device as set forth in claim 19,

wherein the dummy bump is connected to a low impedance portion.

24. A semiconductor device as set forth in claim 19, wherein the dummy bump is provided on a recess formed in the surface of the semiconductor chip.

25. A semiconductor device of a structure in which first and second solid devices are bonded to each other in a face-to-face opposed relation, at least one of the first and second solid devices being a semiconductor chip, the semiconductor device comprising:

an electrical connection portion provided on a front face of the first solid device as projecting therefrom to join the first and second solid devices to each other with a predetermined distance therebetween and to electrically connect the first and second solid devices to each other; and

a dummy connection portion provided on a front face of the second solid device as projecting therefrom to a projection height which is virtually equal to the predetermined distance, and not serving for the electrical connection between the first and second solid devices.

26. A semiconductor device as set forth in claim 25, wherein the second solid device has a connection recess formed in the front face thereof in association

with the electrical connection portion to receive a distal end portion of the electrical connection portion,

wherein the dummy connection portion projects from the front face of the second solid device to a projection height which is virtually equal to a difference between a projection height of the electrical connection portion with respect to the front face of the first solid device and an insertion depth of the electrical connection portion in the connection recess.

27. A semiconductor device of a structure in which first and second solid devices are bonded to each other in a face-to-face opposed relation, at least one of the first and second solid devices being a semiconductor chip, the semiconductor device comprising:

a first electrical connection portion provided on a front face of the first solid device as projecting therefrom for electrical connection between the first solid device and the second solid device;

a dummy connection portion provided on the front face of the first solid device as projecting therefrom and not serving for the electrical connection between the first and second solid devices; and

a second electrical connection portion provided on a front face of the second solid device in association with the first electrical connection portion as

projecting therefrom to a projection height which is virtually equal to a difference in projection height between the first electrical connection portion and the dummy connection portion as measured from the front face of the first solid device, and bonded to the first electrical connection portion for the electrical connection between the first and second solid devices.

28. A semiconductor chip production method for producing a semiconductor chip which is to be bonded to a surface of a solid device and includes an electrical connection portion provided on a front face thereof to be opposed to the surface of the solid device for electrical connection to the solid device and a dummy connection portion provided on the front face thereof and not serving for the electrical connection to the solid device, the method comprising the steps of:

providing an internal interconnection on a semiconductor substrate which serves as a base of the semiconductor chip;

forming a surface protective film over the internal interconnection;

planarizing the surface protective film;

forming an opening in the surface protective film to expose a portion of the internal interconnection; and

forming an electrical connection portion

connected to the internal interconnection via the opening and a dummy connection portion isolated from the internal interconnection by selective plating on the portion of the internal interconnection exposed through the opening and the planarized surface protective film after the surface protective film planarization step and the opening formation step.

29. A semiconductor chip production method for producing a semiconductor chip which is to be bonded to a surface of a solid device and includes an electrical connection portion provided on a front face thereof to be opposed to the surface of the solid device for electrical connection to the solid device and a dummy connection portion provided on the front face thereof and not serving for the electrical connection to the solid device, the method comprising the steps of:

providing an internal interconnection on a semiconductor substrate;

forming a surface protective film over the internal interconnection;

exposing a surface of the internal interconnection from the surface protective film by planarizing the surface protective film by polishing; and

forming an electrical connection portion connected to the surface of the internal interconnection

exposed from the surface protective film and a dummy connection portion isolated from the internal interconnection by selective plating on the surface of the internal interconnection exposed from the surface protective film and the planarized surface protective film.

30. A semiconductor chip production method for producing a semiconductor chip which is to be bonded to a surface of a solid device and includes an electrical connection portion provided on a front face thereof to be opposed to the surface of the solid device for electrical connection to the solid device and a dummy connection portion provided on the front face thereof and not serving for the electrical connection to the solid device, the method comprising the steps of:

providing an internal interconnection on a semiconductor substrate;

forming a surface protective film over the internal interconnection;

planarizing the surface protective film;

forming an opening for partly exposing the internal interconnection and a recess in the planarized surface protective film;

forming a metal film over the surface protective film formed with the recess and the opening; and

removing the metal film except portions thereof formed in the recess and the opening, whereby a dummy connection portion isolated from the internal interconnection and an electrical connection portion connected to the internal interconnection are formed in the recess and in the opening, respectively.

31. A semiconductor chip production method as set forth in claim 30,

wherein the step of forming the dummy connection portion and the electrical connection portion includes the step of polishing a surface of the metal film by a chemical mechanical polishing method, and

wherein the chemical mechanical polishing step is performed until the surface of the surface protective film becomes substantially flush with surfaces of metal film portions in the opening and the recess.